# Design and Analysis of Rectifying and Regulating Rectifier with PWM and PFM modes

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## I. Introduction

Neural stimulators are a key component of neural SoC designed for treating neurological disorders and closing the feedback loop in brain computer interfaces. In this work introduce a wireless power system customized to power a monolithic implantable neural (ECoG) stimulation platform which has a unique power profile. For majority of time period, the stimulator is inactive and the SoC consumes minimal power (~100 μW). During an active stimulation period, a series of 100-200 μs long pulses of high current spaced apart by 2-3 ms are transmitted. This train of pulses is repeated every 200-400 ms. During the conduction of stimulation current, the peak power requirement can vary from 25 mW (1mA@12 V for 50% efficient stimulator) to 1 mW (200μA@12V for 50% efficient stimulator). So, in summary the wireless power system needs to power a load which can varies from 25 mW to 100 μW within 100 μs. These necessities a system which high dynamic range with high efficiency and fast transient response.

Prior wireless power approaches have used an HF rectifier followed by a DC-DC convertor to power these systems using HF wireless power transfer. However, the cascaded systems suffer from low efficiency. Instead, a rectifier which simultaneously regulates is a popular approach to achieve high power conversion efficiency. In [1], authors introduced a 3R rectifier topology. However, this requires external capacitors and diodes which are prohibitive in implanted systems. Additionally, the switching frequencies are low which necessitates bulky filtering capacitor and does not meet the transient requirements. In [2], authors propose an active rectifier with an in-built regulator using a delay line as a control loop operating at 2 MHz carrier frequency. The delay line is a non-linear element which is in a feedback loop to control a rectifier another non-linear element which can lead to unstable designs. The design requires big decoupling capacitors, has only high power mode, does not meeting the transient requirements making it unsuitable to power stimulation platforms.

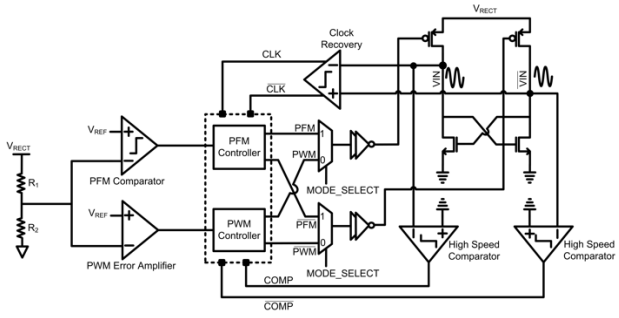


**Figure 1**. Architecture of the proposed rectifying regulator

## II. System Design

In this work, we introduce a 13.56 MHz rectifying regulator topology with low power (PFM) and high power (PWM) modes as shown in Fig. 1. We develop detailed analytical models for design, analysis and optimization of the topology. The architecture consists of a cross coupled NFET switches with PFET active diodes. We show that the cross coupled switch can be oversized to get high efficiency since they are switched by the RF input and hence incur no switch loss. This can be traded-off with smaller PFETs which incur switching losses for constant conduction losses. We develop closed form equations based on 65 nm technology parameters and use it to optimize the size of the switching transistors. To regulate the output voltage in the PWM mode, the conduction angle is controlled every cycle by the feedback loop using the following equation.

$$Vout = \frac{2V_0}{R_s\omega_0}\left[\cos(\omega_0 t_1) - \cos(w_0 t_1 + \Delta t)\right]\left[\frac{T}{R_L} + \frac{2\Delta t}{R_s}\right]^{-1}$$

We use the above equation to synthesize a non-linear transfer function with conduction angle as the input and output voltage as the output for the rectifier. We use this to develop a feedback model and design a rectifier regulator which is stable across different load currents at 2.5V output for 65 nm CMOS process as shown in Fig. 2 with only 1 μF load capacitor (0201 package).

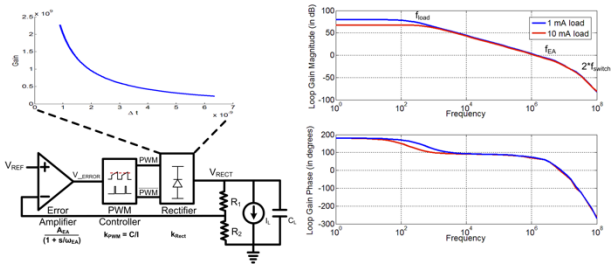


**Figure 2**. Analytical model for the PWM feedback loop. The bode plot shows that system with stable across loads.

Additionally, since in 65 nm CMOS, the control circuitry runs at lower voltage (1 V), we introduce a high dynamic range saw tooth generator using a pseudo charge pump topology. This allows us to cover a range of conduction angle thereby improving the linearity of the system. The feedback loop is designed to be self-synchronized i.e. it recovers the clock from the incoming HF. By doing so it can operate across a range of input frequencies and is compatible with frequency tuning methods. The feedback loop operates at 13.56 MHz switching frequency with high GBW which minimizes settling time.

Finally, for light load duration, we design a PFM mode wherein the feedback loop is set by a static comparator. The output in the PFM mode has lower line regulation but is highly efficient since switching is minimized. The pss analysis for the designed topology agrees well with the developed analytical models.

### References

1. Choi, Jun-Han, et al. "A resonant regulating rectifier (3R) operating at 6.78 MHz for a 6W wireless charger with 86% efficiency." Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International. IEEE, 2013.
2. Lee, Hyung-Min, Hangue Park, and Maysam Ghovanloo. "A power-efficient wireless system with adaptive supply control for deep brain stimulation." Solid-State Circuits, IEEE Journal of 48.9 (2013): 2203-2216.